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LPE technology for power GaAs diode structures

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Abstract. A liquid phase epitaxy technology for deposition of GaAs epilayers on the monocristallic GaAs substrates for high voltage ultra fast power p^+-p-i-n-n^+ GaAs structures has been developed. Proposed technological and hardware solutions of the LPE allow high efficiency of the growing process of diode structures with prescribed ratings and high structural quality of epitaxial layers. A method and technology for the fabrication of GaAs dies for the nanosecond range with reverse voltage up to 1200 V and current up to 100 A in diode chips is introduced. Reverse recovery times down to 20 ns were achieved and could be preserved up to +260 °C.

Key words: LPE technology, crystal defects, process quality, GaAs power diode structures, GaAs static and dynamic characteristics.

1. INTRODUCTION

High frequency, high power and high temperature semiconductor devices have challenged engineers during many decades after their first appearance in the mid of the last century. Most conventional semiconductor power diodes are almost exclusively formed using silicon. Due to the relative maturity of the use of this semiconductor, the ability of conventional power diodes to carry high temperatures, frequencies, currents and to block high voltages is closely approaching the theoretical limit for Si. There are many applications for power diodes that require the ability to carry extra high currents and blocking voltages, like motor control or power supply systems, lighting ballast circuits, power transmission and generation systems, utility power conversion equipment etc. Unfortunately, the overall performance of power diodes, manufactured from Si, is poor for these current or blocking voltage ranges, and the lack of such power diodes represents the primary limitation in realizing circuits and systems for many applications.

Wide band gap semiconductors such as silicon carbide (SiC) and diamond (C) are promising materials for new power devices and theoretically they should bridge the gap between the material limitations and application demands. Diamond and SiC have been specifically known for some time to be excellent semiconductor materials for high temperature and high speed power solutions [1–3]. Unfortunately, real application of the devices, based on wide band gap semiconductor materials, is still strongly limited due to specific crystal growth quality problems [4,5], manufacturing difficulties [6,7] and some other problems, like the availability of suitable high temperature packages etc. In fact, if high voltage diodes that support such high currents and operate at frequencies of 1 to 100 kHz were available, they would revolutionize power utility applications and lead to substantial power savings. Today the semi-wide band gap material GaAs partly fulfils this demand of industrial solutions until the wide band gap materials become available.

This paper is focused on the design and investigation of power GaAs diode structures (chips) based on LPE crystal growth technology developed at Clifton Ltd, Estonia, in cooperation with the scientists from the Department of Electronics, Tallinn University of Technology. First, the method and technology will be shortly described and, secondly, the efficiency of these devices for current blocking and their high speed properties will be demonstrated.

2. METHOD AND TECHNOLOGY

Structures, based on the GaAs high voltage *pn* junction with wide enough low doped base regions can be manufactured today using both LPE and chemical vapour deposition (CVD) technologies. Unfortunately, the CVD technology is principally limited by the thickness of 40 μm for the low doped base region. This is very strong limitation for development of high voltage and high frequency power semiconductor diode structures. For the LPE technology no such a limit exists. Thus a new approach for manufacturing high speed power p^+-p-i-n-n^+ GaAs structures using the LPE technology will be introduced.

The technology, developed at Clifton Ltd, is based on the use of standardized quartz and graphite cassettes for the LPE growth process of GaAs epilayers. During the heating process a slow desorption of oxygen takes place and therefore high quality quartz reactors have been chosen for the LPE process. The thermodynamic analysis of interactions between the quartz reactor, vaporized oxygen and melt gallium showed that the homogenization process of the melt gallium starts before the start of the epitaxial growth process only then when this environment is additionally doped with silicon atoms. The LPE chemical process is described as the joint action of reactions:

$$4\mathrm{Ga}_{(\mathrm{liquid})} + \mathrm{SiO}_{2(\mathrm{solid})} \overset{K_1}{\leftrightarrows} \mathrm{Si}_{(\mathrm{in\ Ga})} + 2\mathrm{Ga}_2\mathrm{O}_{(\mathrm{gas})}, \qquad (1)$$

$$2\mathrm{Ga}_{(\mathrm{liquid})} + \mathrm{SiO}_{2(\mathrm{solid})} \overset{K_2}{\leftrightarrows} \mathrm{SiO}_{(\mathrm{gas})} + \mathrm{Ga_2O}_{(\mathrm{gas})}, \quad (2)$$

$$2\mathrm{Ga}_{(\mathrm{liquid})} + \mathrm{SiO}_{(\mathrm{gas})} \overset{K_3}{\leftrightarrows} \mathrm{Si}_{(\mathrm{in\ Ga})} + \mathrm{Ga_2O}_{(\mathrm{gas})}, \quad (3)$$

$$\mathrm{Si}_{(\mathrm{in\ Ga})} + \mathrm{SiO}_{2(\mathrm{solid})} \overset{K_4}{\leftrightarrows} 2\mathrm{SiO}_{(\mathrm{gas})}, \quad (4)$$

$$4\mathrm{Ga}_{(\mathrm{liquid})} + \mathrm{O}_{2(\mathrm{gas})} \overset{K_5}{\leftrightarrows} 2\mathrm{Ga_2O}_{(\mathrm{gas})}, \quad (5)$$

$$2\mathrm{Ga}_{(\mathrm{liquid})} + \mathrm{H_2O}_{(\mathrm{gas})} \overset{K_6}{\leftrightarrows} \mathrm{Ga_2O}_{(\mathrm{gas})} + \mathrm{H}_{2(\mathrm{gas})}, \quad (6)$$

$$2\mathrm{H}_{2(\mathrm{gas})} + \mathrm{SiO}_{2(\mathrm{solid})} \overset{K_7}{\leftrightarrows} \mathrm{Si}_{(\mathrm{in\ Ga})} + 2\mathrm{H_2O}_{(\mathrm{gas})}. \quad (7)$$

In Eqs. (1)–(7) the participating silicon is dissolved in Ga ($\mathrm{Si}_{(\mathrm{in\ Ga})}$) and takes part in interactive reaction with the quartz reactors. The coefficients K_1–K_7 are determined from the experimental results described, for example, in [8–10]. In accordance with these reactions and adding the vaporized oxygen into the gas environment, we increase the concentration of $\mathrm{Ga_2O}$ and, consequently, the break of the very first initiative reaction will take place, which in turn decreases the concentration of $\mathrm{SiO_2}$ in catalyzing silicon. The silicon drive-in into the gallium during the annealing process is supported through the interaction process between the walls of the reactor and oxygen during the reaction time. The concentration of silicon atoms inside the gallium alloy is connected with the recovery of the reactor quartz by oxygen. The decrease of the amount of vaporized oxygen strongly influences the contamination of the melt gallium with silicon. Therefore during the thermal treatment it is obligatory to follow two contradictory processes – contamination and cleaning of the alloy simultaneously. In [11] it was stated for the first time that GaAs alloy in Ga could lead to the growth of *p*-type GaAs epilayers already before the epitaxial process at certain temperatures, which indeed is the basic idea for the GaAs LPE process. Therefore the only way to drive the profile of doping in the epitaxial process, it is necessary to govern the interaction of the whole system $\mathrm{SiO_2}$–$\mathrm{H_2}$–Ga–$\mathrm{H_2O}$. The patent [12] for the design of the *p-i-n* structure has been followed, where the concept of augmented mass of water in hydrogen environment has been used. The augmented water mass depends on the geometrical dimensions and construction of the reactor and on the concentration of water vapour in hydrogen at the output of the reactor at the annealing temperature; it is described as [13]:

$$M^*_{\mathrm{H_2O}} = [0.344\, q_{\mathrm{H_2O}} (F_{\mathrm{H_2}} t + V_0) L] / (M_{\mathrm{Ga}} d), \quad (8)$$

where $M^*_{\mathrm{H_2O}}$ is the augmented mass of water (mg/g), $q_{\mathrm{H_2O}}$ is the concentration of vapour in hydrogen at the output of the reactor ($\mathrm{mg/m^3}$), $F_{\mathrm{H_2}}$ is the

volume speed of hydrogen flow (m^3/min), t is the annealing time (min), V_0 is the volume of the reactor (m^3), M_{Ga} is the mass of Ga in reactor (mg), L is the length of the reactor (m) and d is the inside diameter (m) of the reactor by which the hydrogen is led into the zone of the alloy.

The 50.8 mm Czochralski or VGF (Vertical Gradient Freeze) substrates GaAs wafers with a concentration of 10^{18}–5×10^{19} cm^{-3} are usually used for the epitaxy. Additional details about the growth process are presented in [14,15]. Our experiments also show that during the epitaxial growth the development of the elongated *i*-region takes place, and we guess that this is related to the properties of the silicon catalist in reactor. In the beginning of the epitaxial growth, the silicon forms connections with the vacancies or oxygen atoms, and shows that the acceptor properties are generating low energy levels near the valence band. In the case of inversion type conductivity of the epitaxial layer, the silicon atoms continually start to form nodes inside the subnet of gallium and through this process to increase the concentration of low donor levels near the bottom of the conductivity band. The *i*-layer presumably will be strongly compensated by the silicon from different subnets of GaAs. This statement is supported by the results from photoluminescence experiments, where the peak of irradiation appears on 1.507 eV at 87 K. This fixation indicates the existence of a jump of electrons from low energy donor level into the valence band, and the process is very extensive for both *n*- and *p*-solutions.

By the development of power structures, it is important to ensure maximum reverse breakdown voltage, but at the same time the losses must be kept on the minimum level at high forward current values. The forward losses can be decreased by decreasing the width of the narrow base region and increasing the lifetime of minority charge carriers; however, this leads to the decreasing of the concentration of deep level centres. From the other hand, we have to keep in mind that the increase of speed of the devices depends directly on the decrease of the minority charge carriers' lifetime. Thus here we have a clear conflict situation from the point of view of manufacturing and realization of material properties and device characteristics. Therefore the aim of our attempts by the LPE fabrication of GaAs epilayers was to keep the concentration of deep level centres as low as possible. We managed to reach a situation, where permanently only two main deep level centres are available (A-level with the activation energy about $E_V = 0.41$ eV and B-level with the activation energy about $E_V = 0.68$ eV) and their concentrations are pretty equal in the epitaxial layer; therefore these centres are like a fingerprint of the LPE technology in general. Our experiments show also that a similar result can be achieved for *p*-*i*-*n* structures as well. The length of the work zone of the horizontal epitaxial growth equipment in standardized industrial applications is about 80 cm. This dimension limitation allows simultaneous handling of about 60 GaAs wafers. We have changed the manufacturing process and gas handling system so that simultaneously three growth equipments can be handled in parallel, which increases the yield for three times. Figure 1 shows as an example the connection scheme of two epitaxial growth equipments.

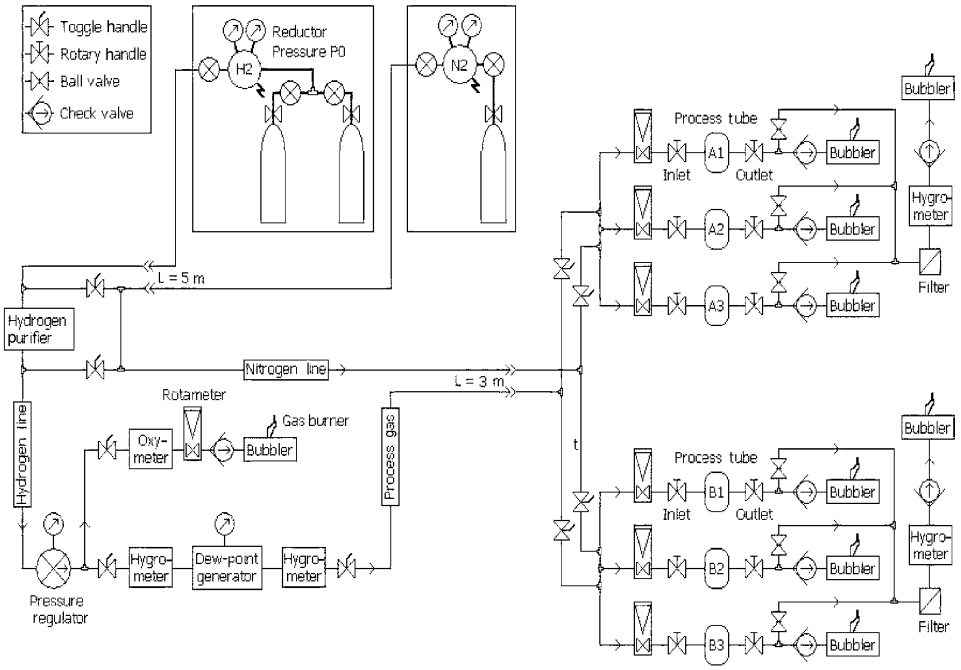

Fig. 1. Description of the gas distribution system for LPE for two parallel equipments.

The distribution of doping concentration in epilayers depends significantly on the concentration level of Zn in the substrate and this in turn has influence on the width of the growing *p*-layer; our experiments show that Zn plays a significant role in the growth process of the *p*-epilayer.

3. RESULTS

The experiments show very clearly that the most important role on LPE growth of the *p*-*i*-*n* structures on p^+-substrates plays the crystal quality of the p^+-GaAs substrate ityself. The strongest influence on the quality of the growing *p*-*i*-*n* structures has the possible transmission of dislocations from the p^+-substrate into the epilayer. The p^+-substrates used in this particular applications were grown with the method of Chochralski with the dislocation density of $(1–5) \times 10^4$ cm^{-2}. Our experiments show that the substrates having the form of the so-called Mercedes-type (Fig. 2a), the dislocation density in the epilayers reached the values of 10^6 cm^{-2} or even higher. The dislocations reach the depth of 30 μm in epilayers and the majority of them in epilayers have already the form of a half loop.

When the Mercedes-type dislocations in the substrate have no catastrophic consequences on the quality of the epilayers, the technology-introduced possible

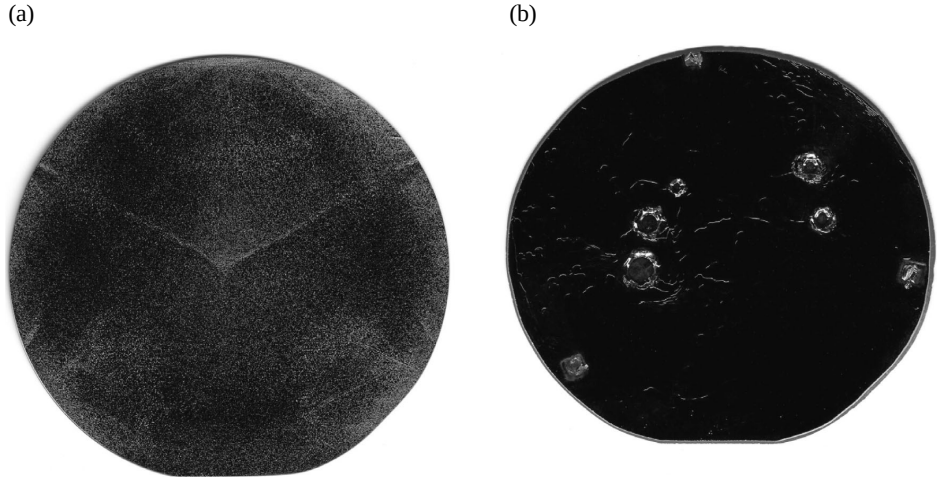

Fig. 2. GaAs wafer surface: (a) emerge of "Mercedes-type" dislocations on surface of p^+-substrate; (b) technology induced craters in epilayers caused by the wrong movement of the hydrogen bubble.

hydrogen bubble defects destroy the high quality yield of the process (Fig. 2b). Methods for avoiding the appearance of such defects have been developed and applied and described elsewhere [14]. The surface of the epilayers after the growth process can typically be divided into four classes: mirror smooth, gradual smooth, waved smooth and hilly smooth. Also combinations of the described surface types are possible. Figure 3a shows, for example, the gradual-hilly smooth surface of the epilayer, and Fig. 3b the mirror smooth surface of the *p-i-n* surface.

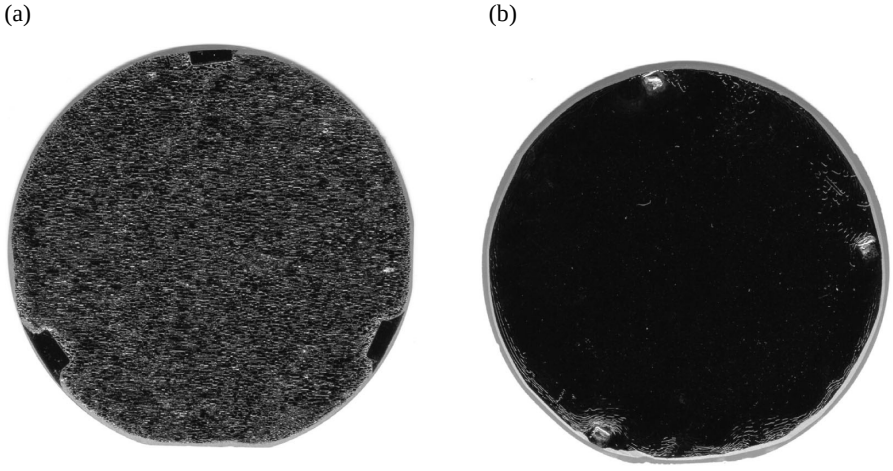

Fig. 3. GaAs wafer surface: (a) the gradual-hilly surface of the p^+-*p-i-n*, grown on the surface with 2 deg deviation from the (100) orientation; (b) typical mirror surface of the p^+-*p-i-n* surface.

The emergence of the gradual-hilly smooth surface is straightforwardly connected with the aberrancy of the substrate orientation and follows directly from the breakup of the substrate orientation, which makes worse the quality of the epilayer. Forming of the gradually smooth surface takes place due to the growth of the microsteps on the surface of the substrate. The dependence of the epilayer quality on cassettes and their material and dimensions was not observed by the growth process (Fig. 3a). To insure the best quality of the surface of the epitaxial layer, the orientation deviation from the singular crystallographic surface must be as small as possible. Our practical results show less than 0.5 deg deviation from the (111)B surface. The fluctuation in height of the *p-i-n* broken surface structure can reach some micrometers. The larger the slot between substrates in the epitaxial process, the higher can be the fluctuation of the broken structure of the surface.

Figure 4a shows the prepared high voltage GaAs chips with the dimensions of 3 × 3 mm. The ohmic contacts have been sputtered using standard evaporation technology.

The diode structures, based on in Fig. 4a shown chips, have the p^+-*p*-*i*-*n*-n^+ structure and they are able, after passivations of the surface and phasing of the sides, to manage reverse blocking voltage up to 1200 V. Figure 4b shows the real cross-section of the power GaAs diode chip. The Clifton Ltd produces on this base three different diode structures, determined by reverse recovery time t_{rr} and forward voltage V_F as follows: **DS** (superfast) – $t_{rr} \le 35$ ns, $V_F \le 2.1$ V; **DU** (ultrafast) – $t_{rr} \le 50$ ns, $V_F \le 1.8$ V; **DF** (fast) – $t_{rr} \le 75$ ns, $V_F \le 1.7$ V. The explanatory picture is presented in Fig. 5.

The measured data are shown in Table 1 (with the conditions: $I_F = 15$ A, current change rate $\mathrm{d}i/\mathrm{d}t = -800$ A/μs, $V_{RRM} = 400$ V, and cathode contact area dimensions ($d \times d$) are 2.6 × 2.6 mm). In Table 1, T_j is the junction temperature.

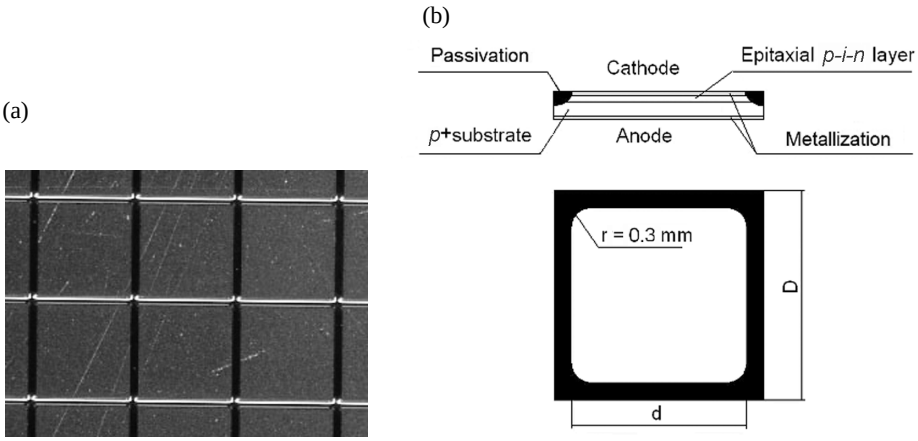

Fig. 4. The GaAs chip: (a) the 3 × 3 mm GaAs chips for high speed power diode structures; (b) the cross-section of the real GaAs power diode chip.

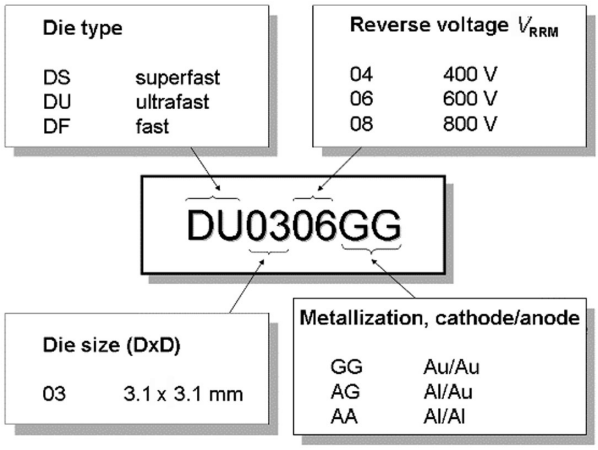

Fig. 5. The explanatory picture for the GaAs power diode chips.

Table 1. Typical values of electrical parameters for diode structures

Die code	V_{RRM}, V	t_{rr}, ns	Max V_F at 15 A, V			Max I_R, mA		Max C_j at 200 V, pF
		T_j, °C						
		25–260	25	175	260	175	260	25
DS0304GG DS0306GG DS0308GG	400 600 800	35	2.1	2.3	2.5	0.3	1.0	22
DU0304GG DU0306GG DU0308GG	400 600 800	50	1.8	2.0	2.2	0.3	1.0	22
DF0304GG DF0306GG DF0308GG	400 600 800	75	1.7	1.9	2.0	0.3	1.0	22

It is clearly seen from Table 1 that the diodes with smaller reverse recovery time (t_{rr}) have higher forward voltage (V_F) drop compared to other samples. The reason has been shortly explained in the previous section of this paper. The chips with the reverse blocking voltage (V_{RRM}) 1200 V have the same area as the structures with lower forward currents and with the blocking voltage of 600 V. The most important advantage of GaAs diodes compared with Si diodes is the high temperature capability, when the GaAs diode junction temperature is allowed to rise up to +260 °C, and the reverse recovery time practically does not depend on the junction temperature. Figure 6 presents typical curve for the dependence of the current I on the reverse recovery time, based on the data of Table 1.

Figure 7 shows typical forward and reverse static characteristics for the 600 V GaAs structures at two different temperatures.

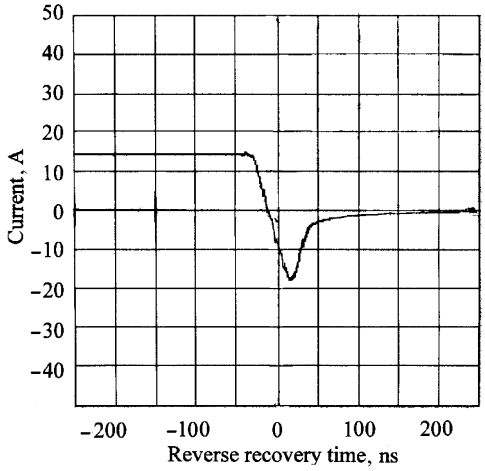

Fig. 6. Typical transition process curve, dependence of the current on the reverse recovery time. Test conditions: current change rate d*i*/d*t* = –800 A/μs, V_{RRM} = 400 V, T_j = 25 °C.

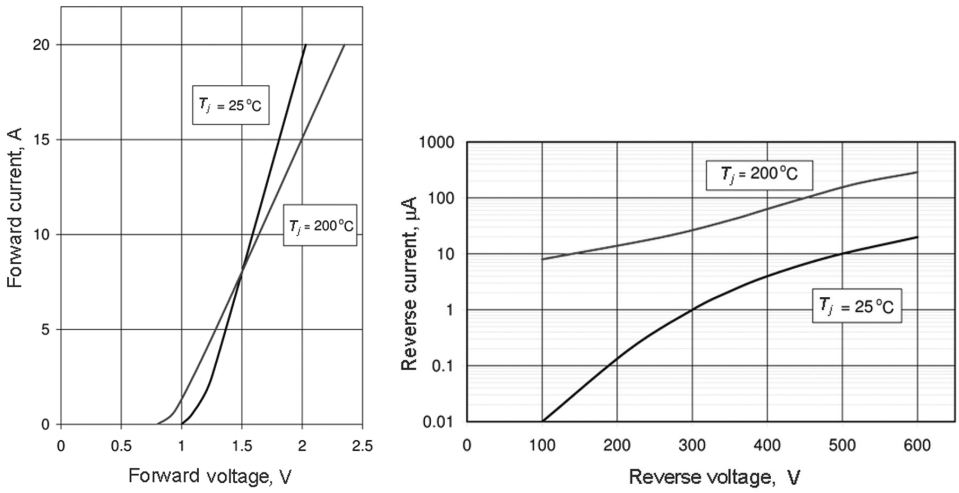

Fig. 7. Measured forward and reverse static characteristics of 600 V GaAs structures.

Figure 8 shows important measured dynamic and static properties of GaAs power diode chips at different junction temperatures. Figure 8a explains clearly the behaviour of the depletion layer inside the structure. The relatively lowly doped epilayer fixes quite clearly the depletion layer boundary at the voltages over 50 V, which is expressed as almost constant capacitance by higher applied reverse voltage. The different reverse recovery characteristics tell us about the good physical properties of LPE based GaAs chip technology over a wide range of (d*i*/d*t*).

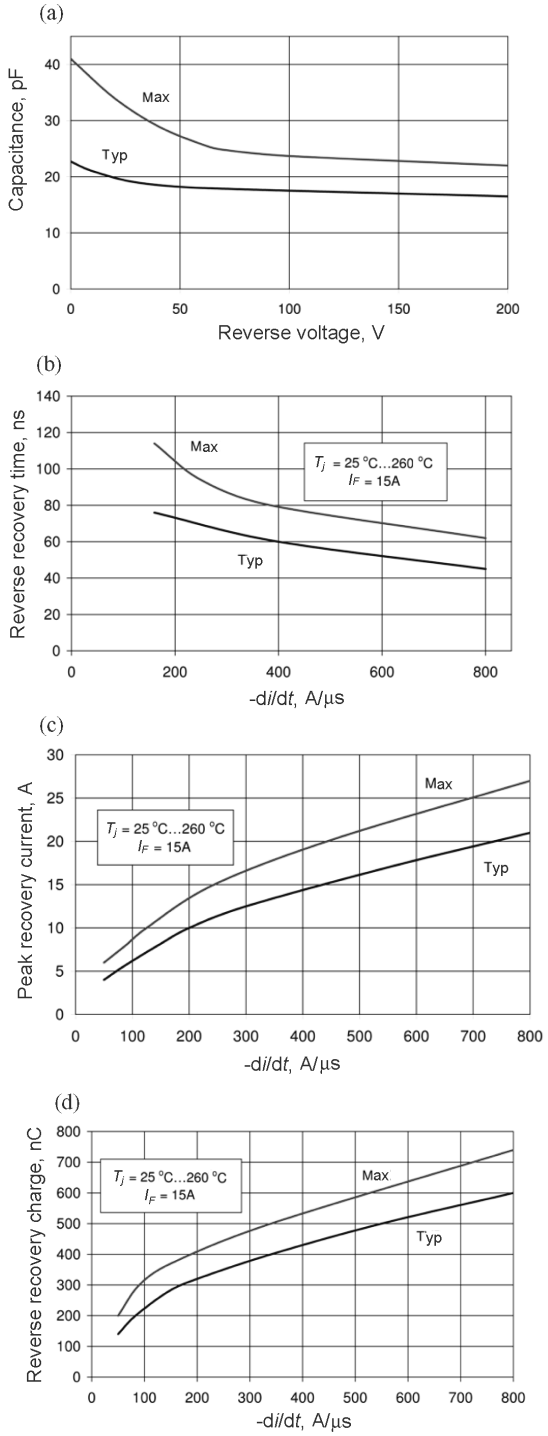

Fig. 8. Static and dynamic parameters of GaAs power diode chips (Max – maximally allowed values, Typ – typical values).

4. CONCLUSIONS

We have shortly presented a novel LPE technology for manufacturing high speed power diode structures. Two important conclusions are to be pointed out.

- A dependable industrial 50.8 mm wafer technology has been developed for GaAs p^+-p-i-n-n^+ diode structures, based on the LPE method.
- The manufactured diodes have excellent electrical characteristics at high ambient temperature, and the reverse blocking voltage reaches 1200 V.

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Vedelikepitaksia tehnoloogia GaAs-jõudioodide valmistamiseks

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On kirjeldatud vedelikepitaksia tehnoloogiat GaAs-epitaksiaalkihtide valmistamiseks monokristallilistele GaAs-alustele. Väljatöötatud tehnoloogia ja selle riistvaraline realisatsioon võimaldab kasvatada monokristallilistele GaAs-alustele kõrge kvaliteediga epitaksiaalkihte, mis omakorda võimaldab valmistada ülikiireid (vastutaastumisaeg on suurusjärgus 20 ns) kõrgepingelisi (vastupinge kuni 1200 V) jõudioodide kiipe (lubatud pärivool kuni 100 A). Valmistatud näidised säilitavad oma elektrilised omadused ka kõrgetel temperatuuridel (siirdetemperatuuril kuni +260 °C).